In the Claims:

This listing of claims replaces all prior versions.

1.   (Previously presented) A system comprising:

a processor that executes logical or arithmetic operations;

a plurality of register bank blocks used as special function registers by the processor during the execution of the logical or arithmetic operations and,

a register bank block decoder circuit for activating one and only one of the plurality of register bank blocks, the register bank block decoder circuit responsive to interrupt event operations for selecting the one of the plurality of register bank blocks for being activated, where different interrupt event operations result in selection of different ones of the plurality of register bank blocks.

2.   (Previously presented) A system according to claim 1, further comprising:

a memory circuit for storing of a first program stream and for storing of a second program stream, wherein the processor utilizes a first register bank block from the plurality of register bank blocks during execution of the first program stream, and upon the occurrence of an interrupt resulting from an interrupt event associated with the second program stream, the processor executes the second program stream utilizing a second register bank block, the second register bank block different and logically isolated from the first register bank block.

3.   (Original) A system according to claim 2, wherein the second program stream has a higher interrupt priority than the first program stream.

4.   (Previously presented) A system according to claim 1, further comprising:

an input data bus and,

an input switching circuit coupled to the plurality of register bank blocks and having a selection input port for receiving a register bank block selection signal from the register bank block decoder circuit, the input switching circuit for activating one of the plurality of register bank blocks in dependence upon the register bank block selection

signal, the activated one of the plurality of register bank blocks being coupled to the input data bus.

5.   (Previously presented) A system according to claim 4, wherein the input switching circuit is a multiplexer circuit.

6.   (Previously presented) A system according to claim 4, further comprising:
        an output data bus; and,
        an output switching circuit coupled to the plurality of register bank blocks and having a selection input port for receiving the register bank block selection signal from the register bank block decoder circuit, the output switching circuit for switchably coupling the activated one of the plurality of register bank blocks to the output data bus.

7.   (Previously presented) A system according to claim 6, wherein the output switching circuit is a multiplexer circuit.

8.   (Previously presented) A system according to claim 6, further comprising a circuit for storing and retrieving of register bank block selection data derived from the register bank block selection signal, the register bank block selection data indicative of a pre interrupt switch state, wherein upon terminating of an interrupt event, the input switching circuit and the output switching circuit are provided with a pre interrupt register bank block selection signal derived from the stored register bank block selection data.

9.   (Previously presented) A system according to claim 8, wherein the state of the circuit for storing and retrieving of the register bank block selection data is based on interrupt priority.

10.   (Original) A system according to claim 6, wherein the register bank block selection signal is based solely on interrupt priority.

11.   (Previously presented) A system according to claim 1, wherein a first register bank block from the plurality of register bank blocks is concurrently enabled along with a second different register bank block from the plurality of register bank blocks, the second different register bank block independently addressable from the first register bank block.

12.   (Previously presented) A system according to claim 1, further comprising a debug bank select register coupled to the register bank block decoder circuit, the debug bank select register for providing access to program stream data stored within the plurality of register bank blocks during a step of debugging.

13.   (Previously presented) A method of switching processing resources in a data processing system comprising the steps of:
    providing a plurality of register bank blocks;
    utilizing a first register bank block from the plurality of register bank blocks 120, as special function registers during execution of logical or arithmetic operations;
    receiving of an interrupt request for initiating an interrupt event;
    determining if the interrupt request is to be fulfilled, and if so, then: selecting a second register bank block from the plurality of register bank blocks , the selected second register bank block in isolation from the first register bank block; and,
    utilizing the second register bank block from the plurality of register bank blocks as special function registers during execution of logical or arithmetic operations.

14.   (Previously presented) A method according to claim 13, wherein a first program stream is provided for utilizing of the first register bank block and a second program stream is provided for utilizing the second register bank block.

15.   (Previously presented) A method according to claim 14, wherein the first program stream has a lower interrupt priority than the second program stream, the interrupt priority used in the step of determining whether to fulfill the interrupt request.

16.   (Previously presented) A method according to claim 14, wherein a processor executes the first and second program streams.

17.   (Previously presented) A method according to claim 16, further comprising the steps of:

      halting execution of the second program stream;

      selecting the first register bank block; and,

      resuming execution of the first program stream.

18.   (Previously presented) A method according to claim 17, wherein executing the instructions of the second program stream takes place without altering the contents of the first register bank block in suspended use by the first program stream.

19.   (Previously presented) A method according to claim 14, further comprising the step of:

      providing a memory circuit having a first memory region for storing of program stream data related to the first program stream.

20.   (Previously presented) A method according to claim 14, wherein the first and second program streams have stored therein instruction data for storing and restoring of register bank block contents.

21.   (Previously presented) A storage medium having data stored thereon, the data for implementation of a processing system comprising:

      first instruction data for providing a plurality of register bank blocks that are used as special function registers during execution of logical or arithmetic operations and,

      second instruction data for providing a register bank block decoder circuit for activating one of the plurality of register bank blocks in isolation, the register bank block decoder circuit responsive to interrupt event operations for selecting the one of the plurality of register bank blocks for being activated, where different interrupt event operations result in selection of different ones of the plurality of register bank blocks.